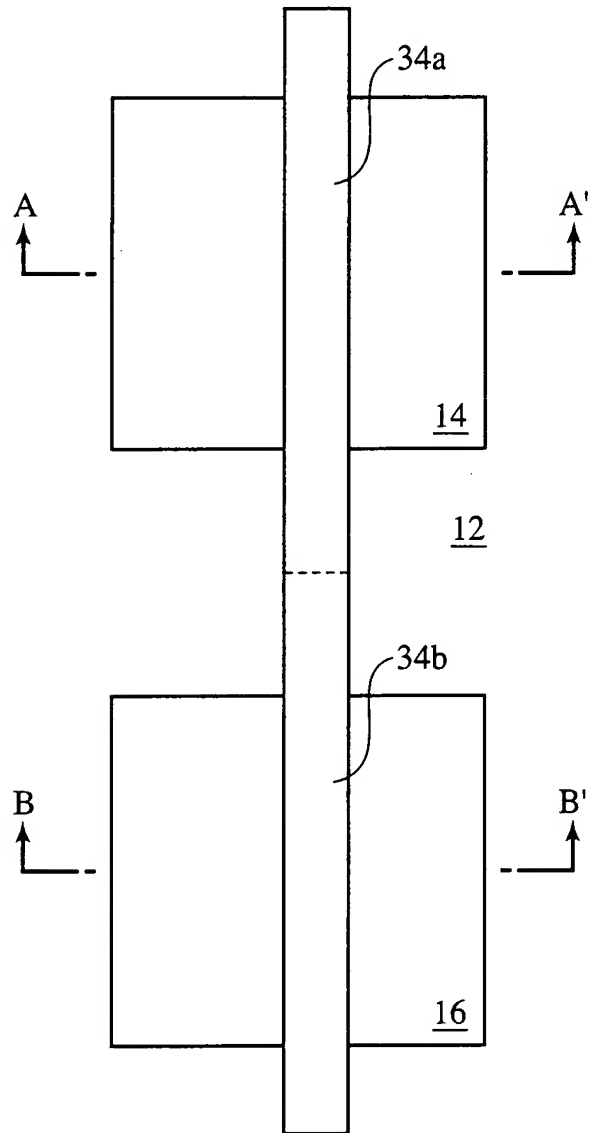
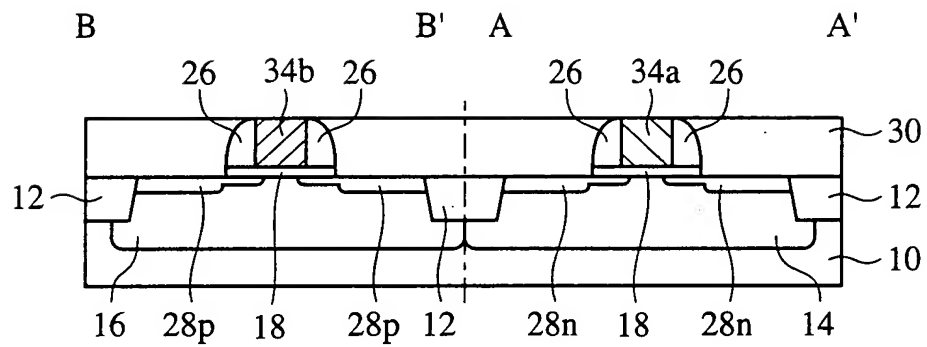


1/27

FIG. 1





3/27

FIG. 3A

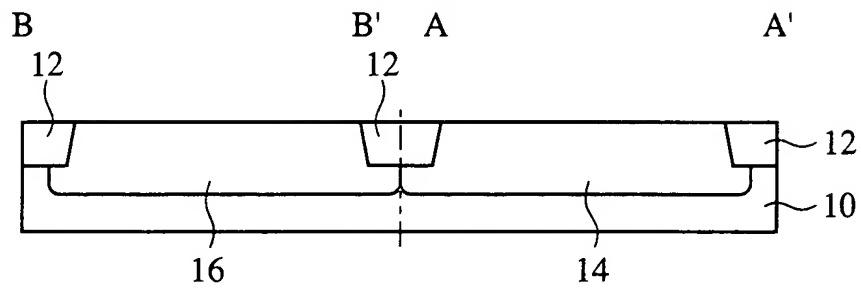


FIG. 3B

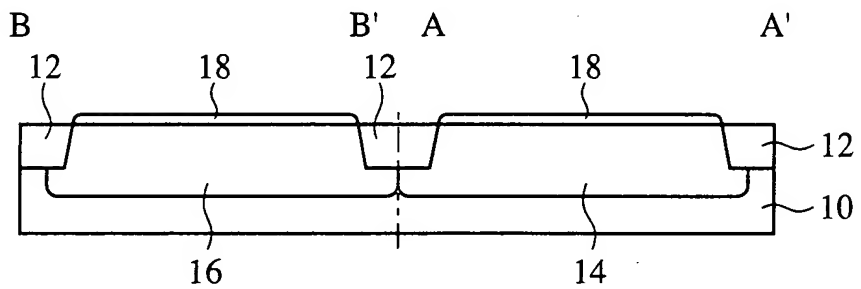
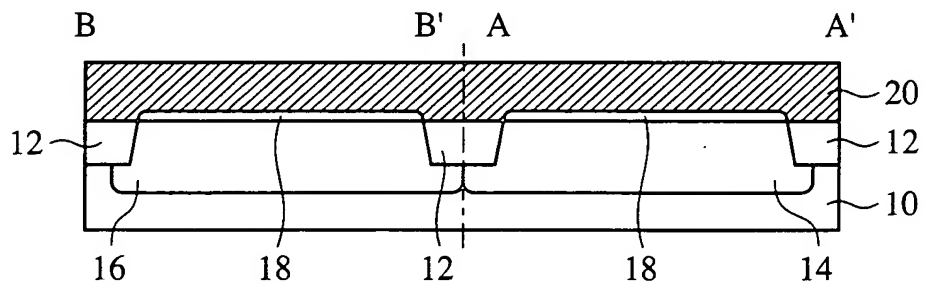


FIG. 3C



4/27

FIG. 4A

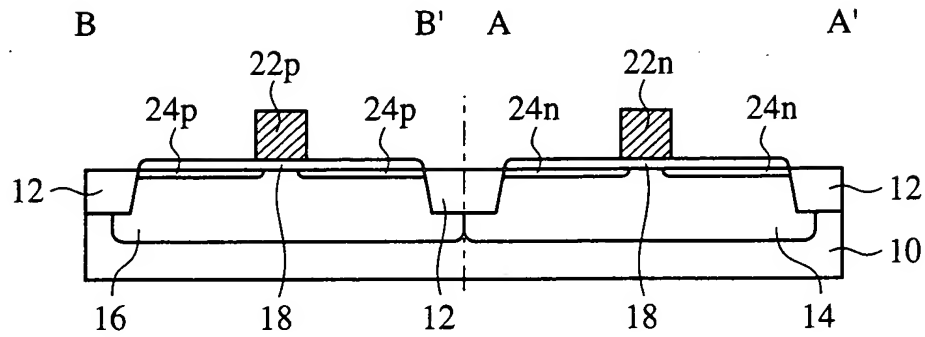


FIG. 4B

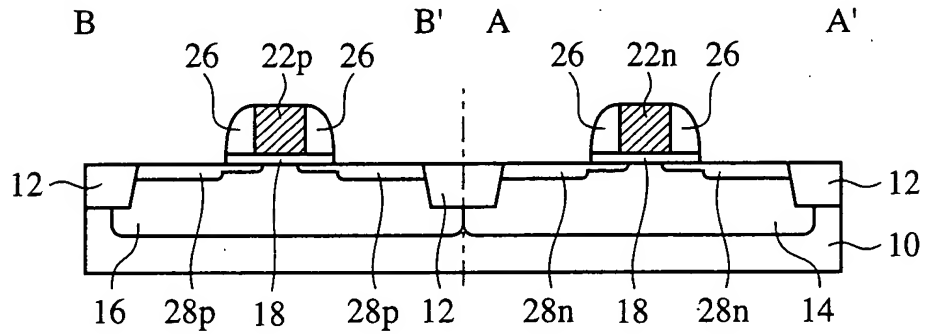
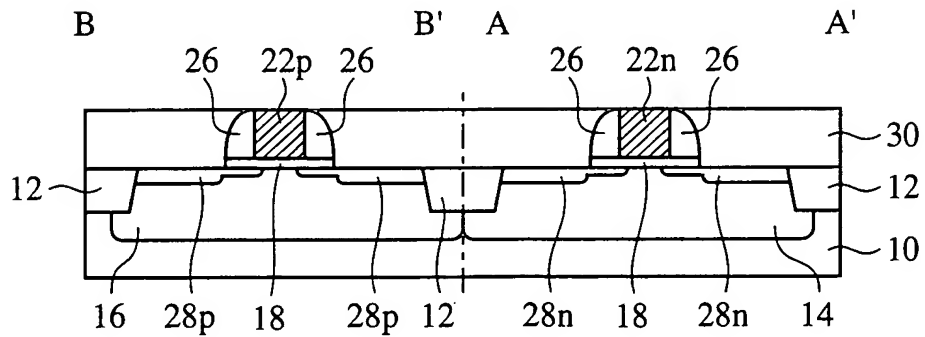


FIG. 4C



5/27

FIG. 5A

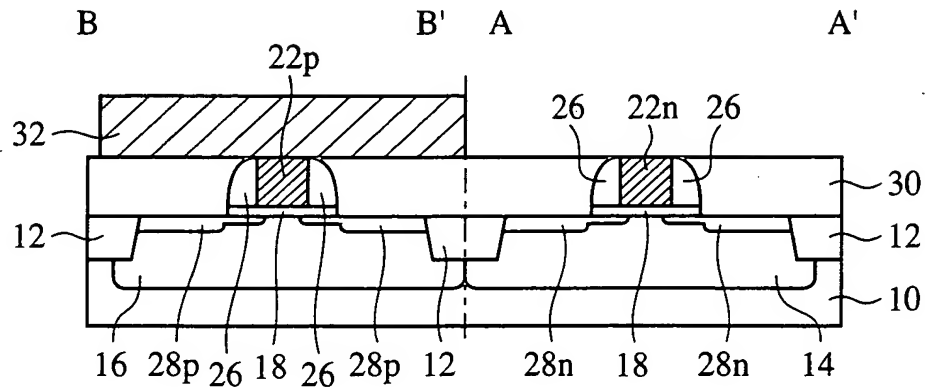


FIG. 5B

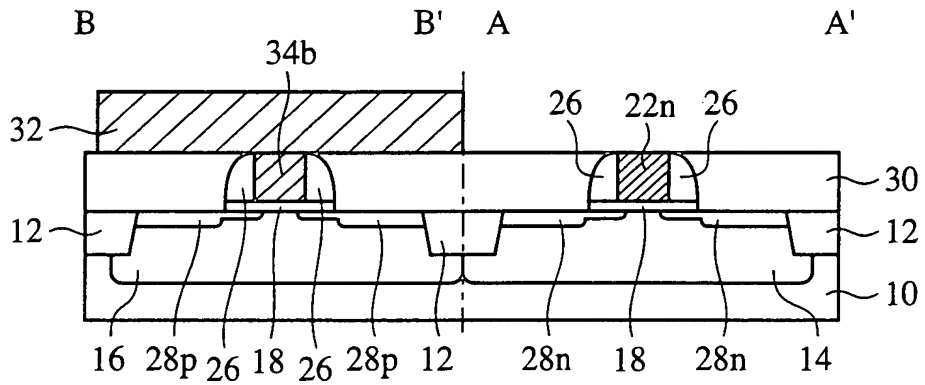
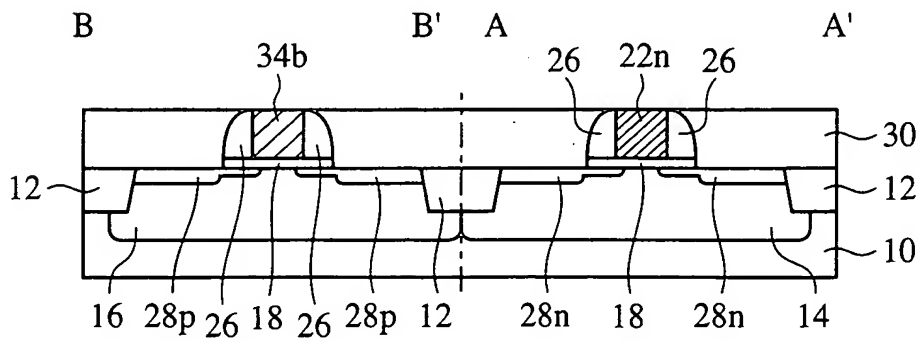


FIG. 5C



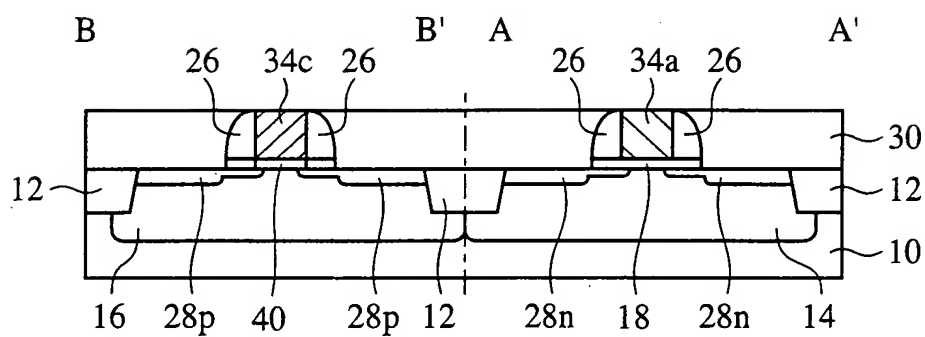
[illegible]

This cross-sectional view shows a second embodiment of the semiconductor device. It features a substrate 10 with a first conductive layer 12. A second conductive layer 14 is formed on the first conductive layer 12, with a central portion 16. A second insulating layer 18 is formed on the second conductive layer 14, with a central portion 20. A second conductive layer 26 is formed on the second insulating layer 18, with a central portion 28n. A second insulating layer 30 is formed on the second conductive layer 26, with a central portion 32. A second conductive layer 34a is formed on the second insulating layer 30, with a central portion 34b. A second conductive layer 36 is formed on the second insulating layer 30, with a central portion 38. The second conductive layer 34a is formed on the second insulating layer 30, with a central portion 34b. The second conductive layer 36 is formed on the second insulating layer 30, with a central portion 38. The second conductive layer 34a is formed on the second insulating layer 30, with a central portion 34b. The second conductive layer 36 is formed on the second insulating layer 30, with a central portion 38.

[illegible]

7/27

FIG. 7



8/27

FIG. 8A

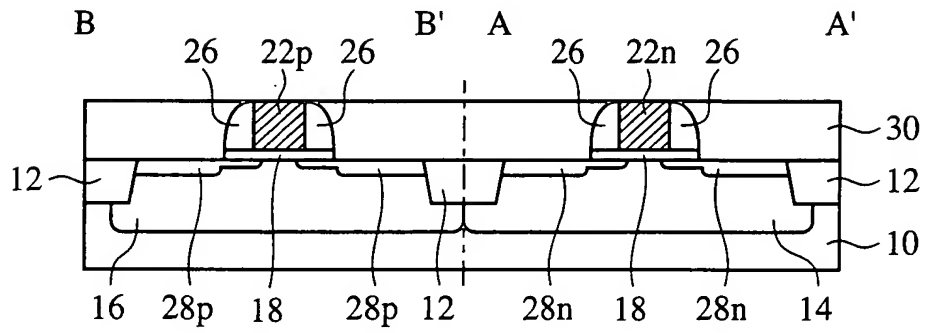


FIG. 8B

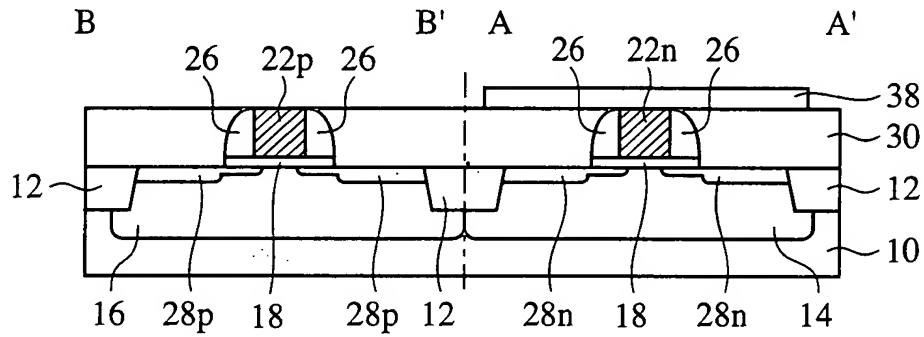
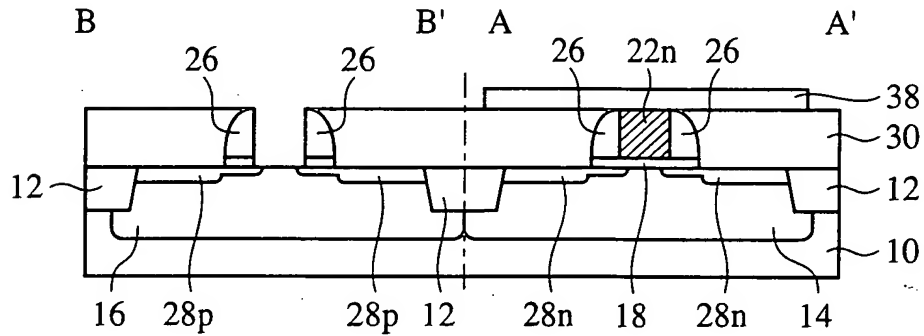


FIG. 8C





9/27

FIG. 9A

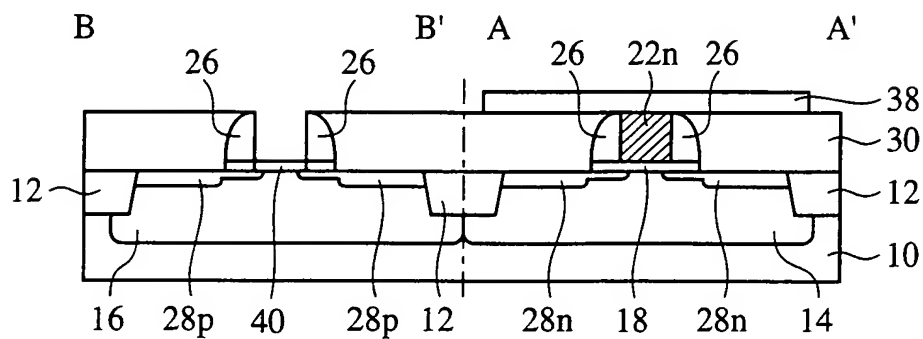


FIG. 9B

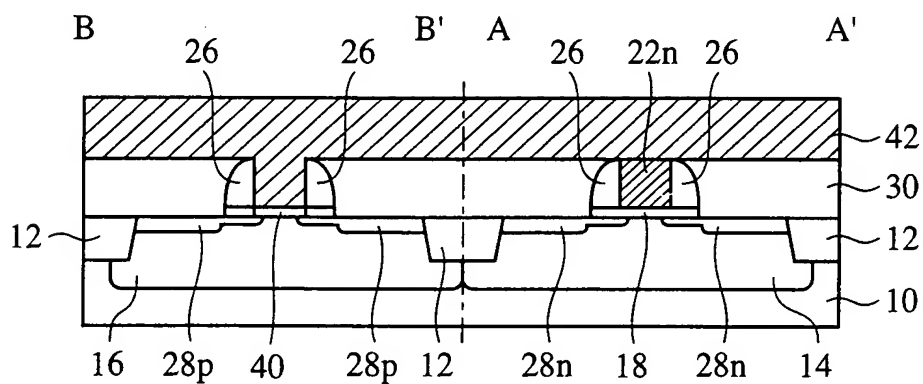
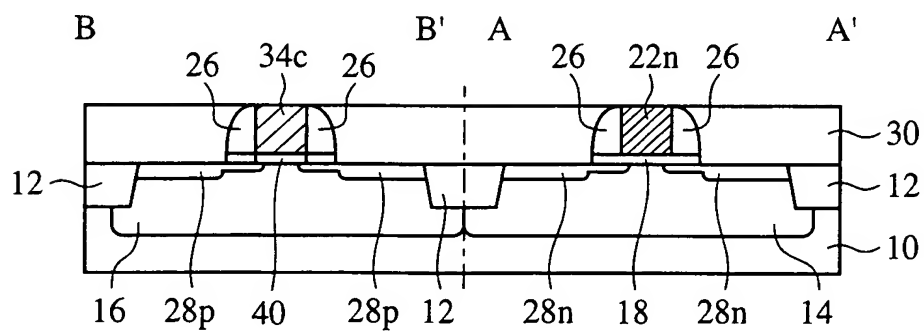


FIG. 9C



10/27

FIG. 10A

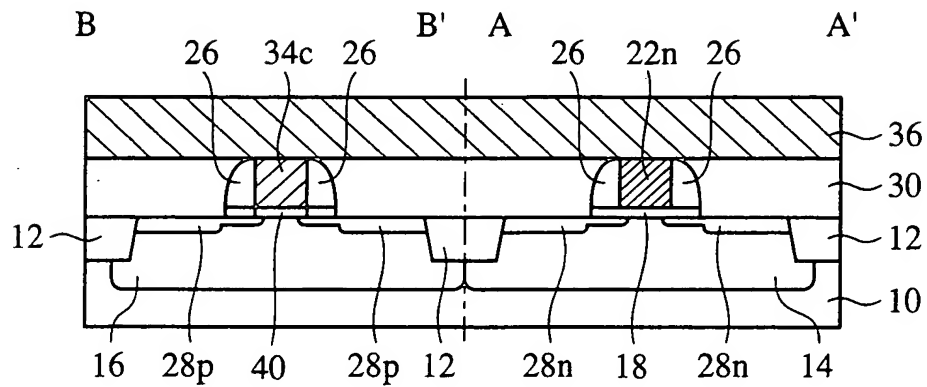


FIG. 10B

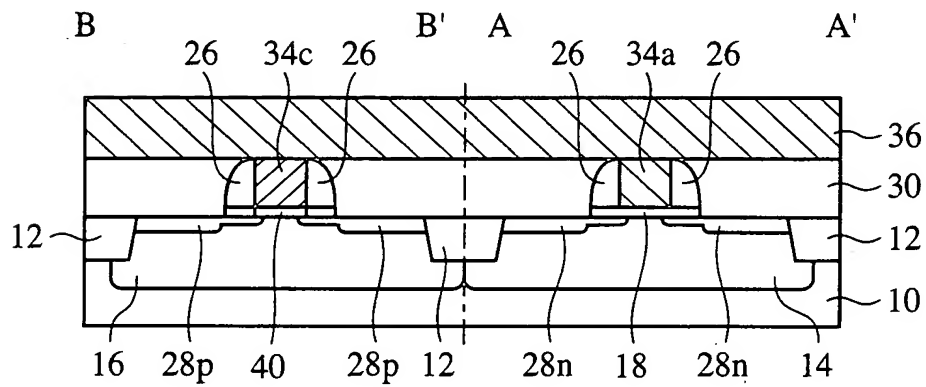
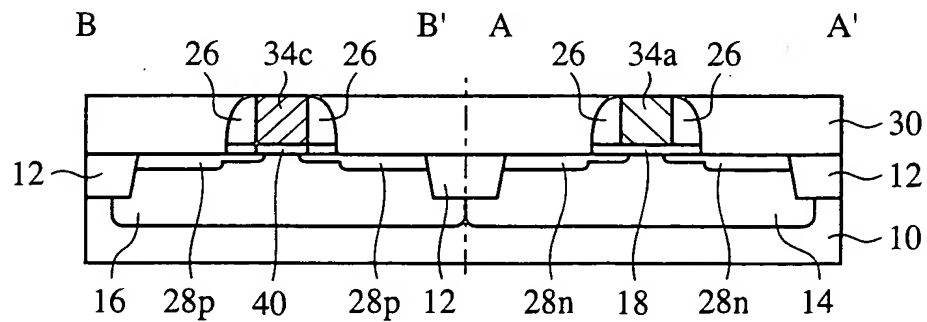
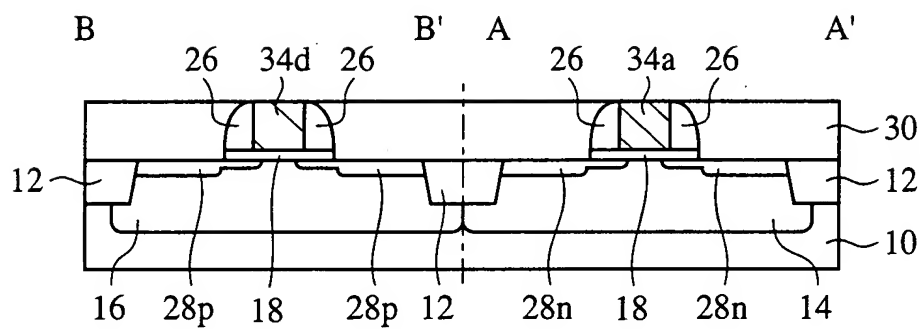


FIG. 10C



11/27

FIG. 11



12/27

FIG. 12A

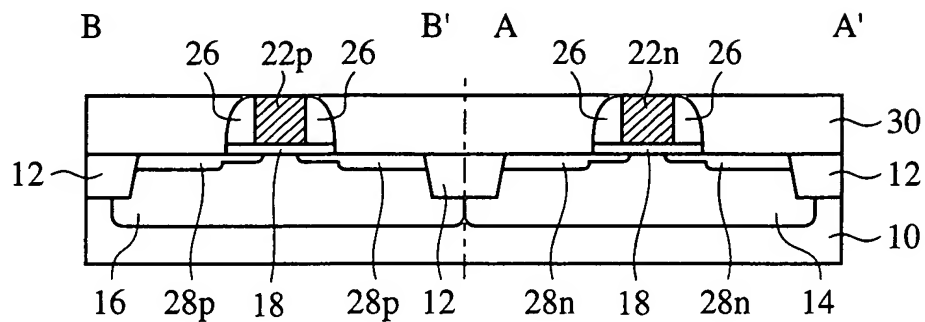


FIG. 12B

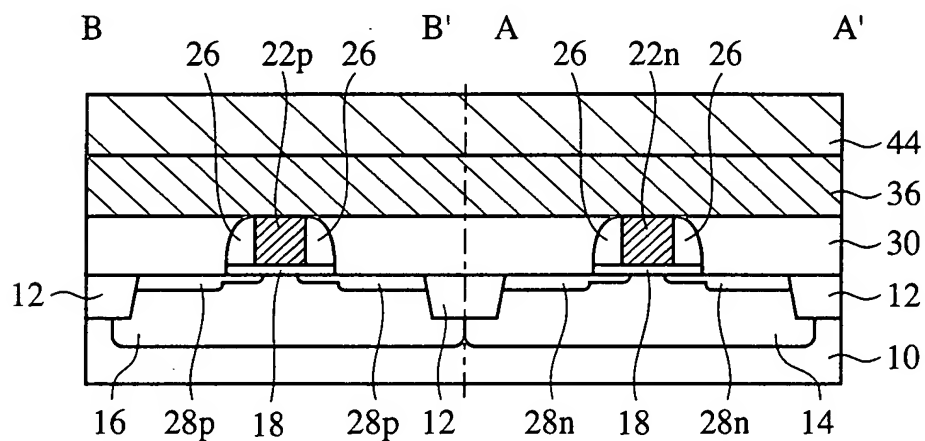
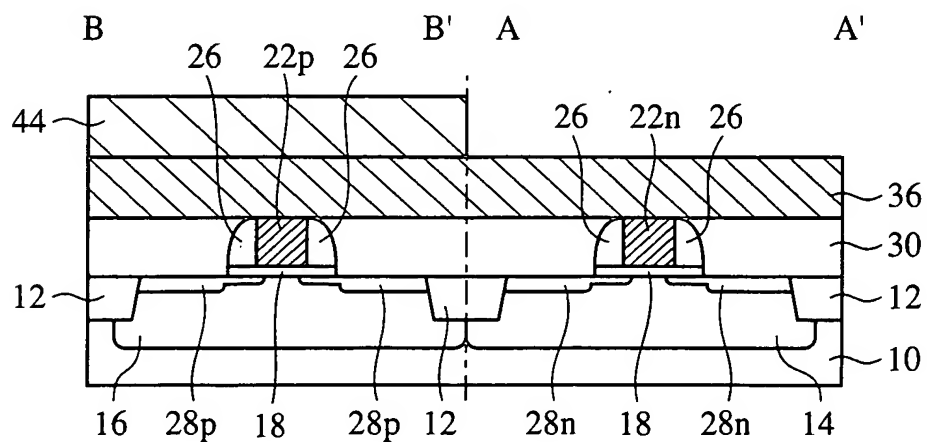


FIG. 12C



13/27

FIG. 13A

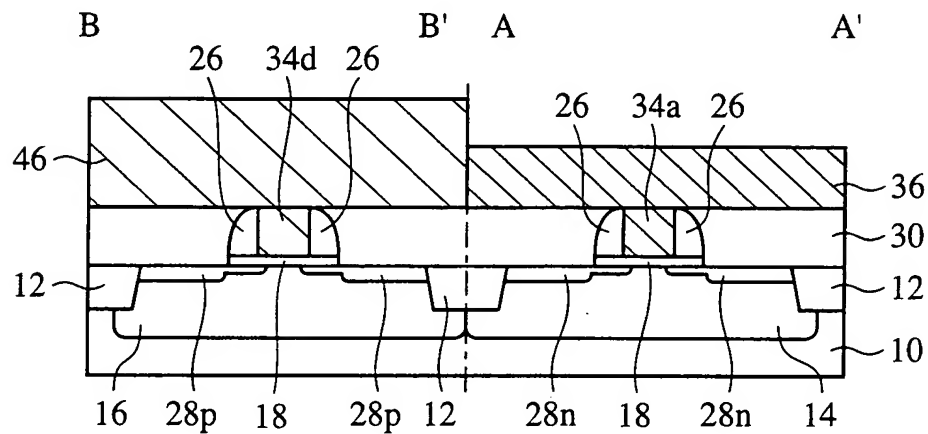
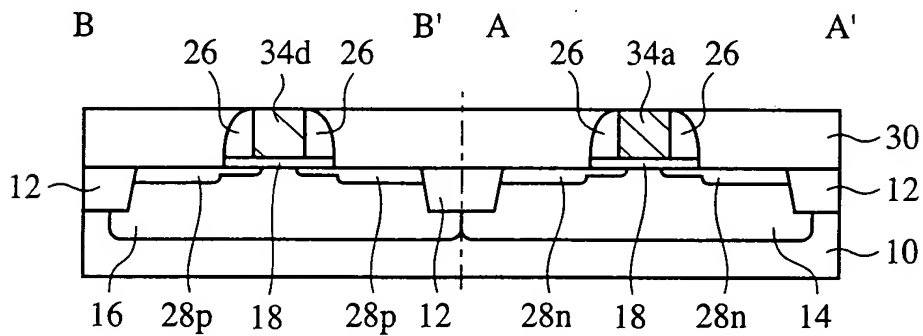
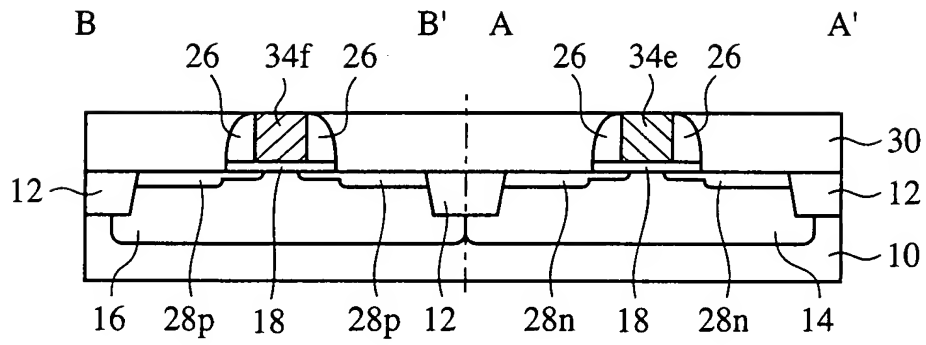


FIG. 13B



14/27

FIG. 14



15/27

FIG. 15A

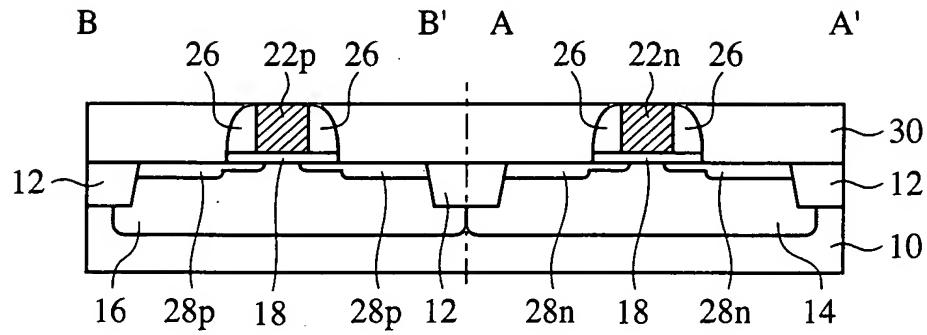


FIG. 15B

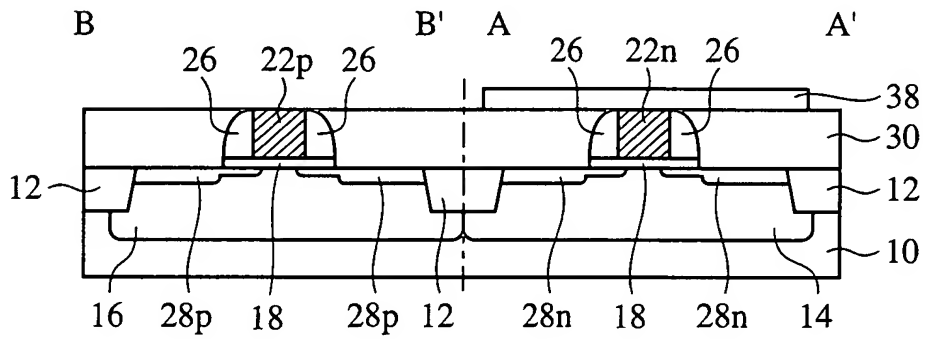
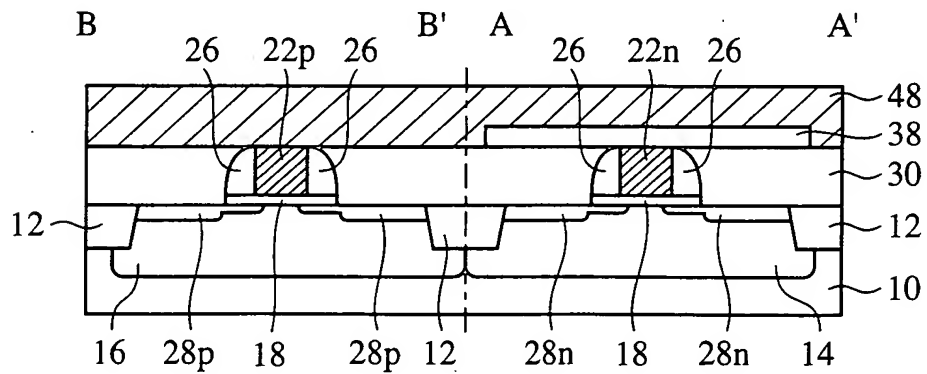


FIG. 15C



16/27

FIG. 16A

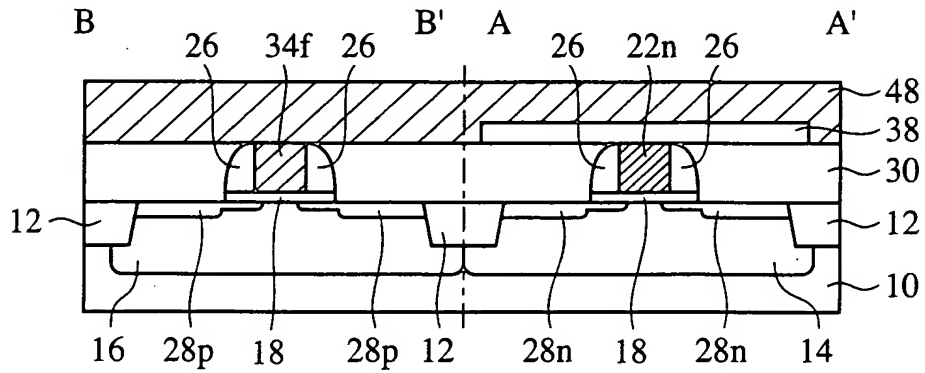


FIG. 16B

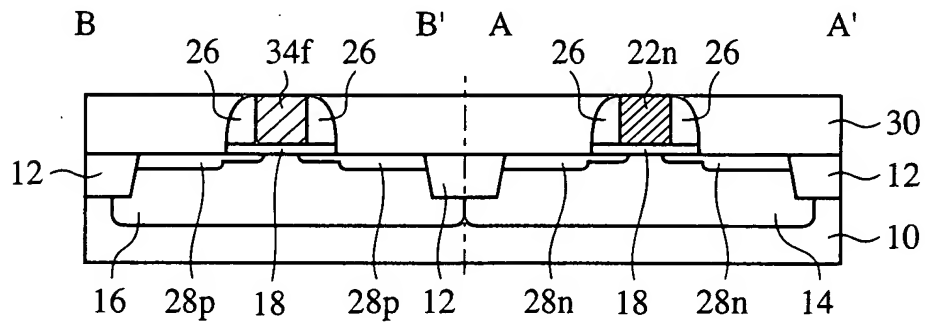
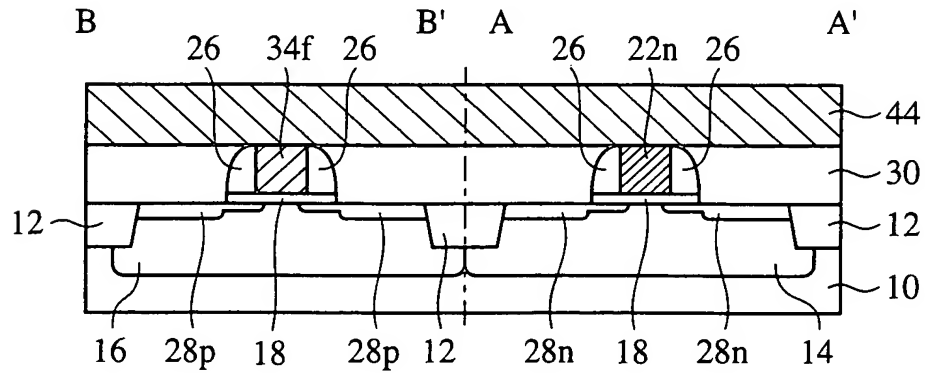
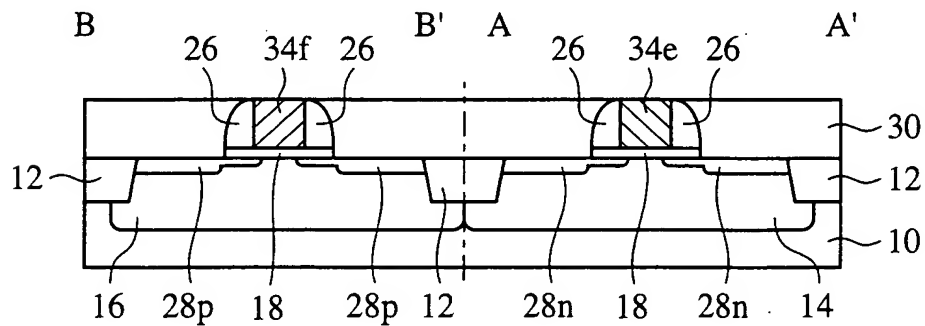


FIG. 16C

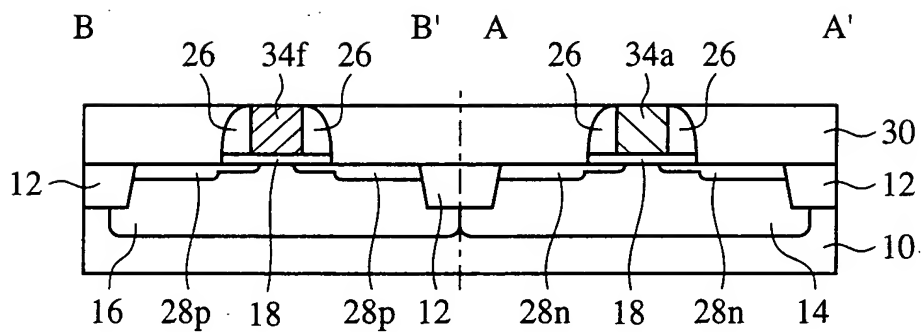






18/27

FIG. 18



19/27

FIG. 19A

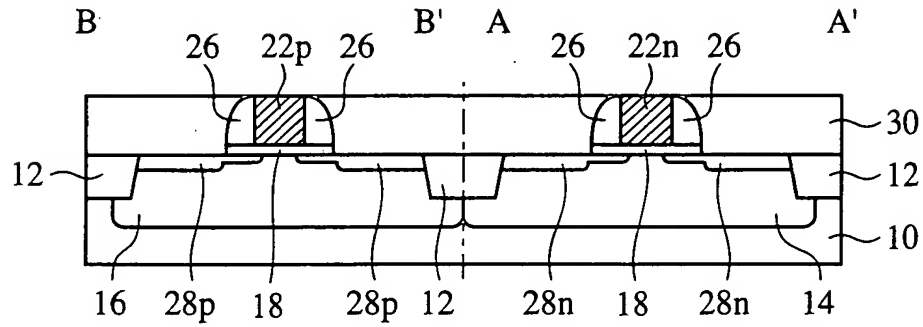


FIG. 19B

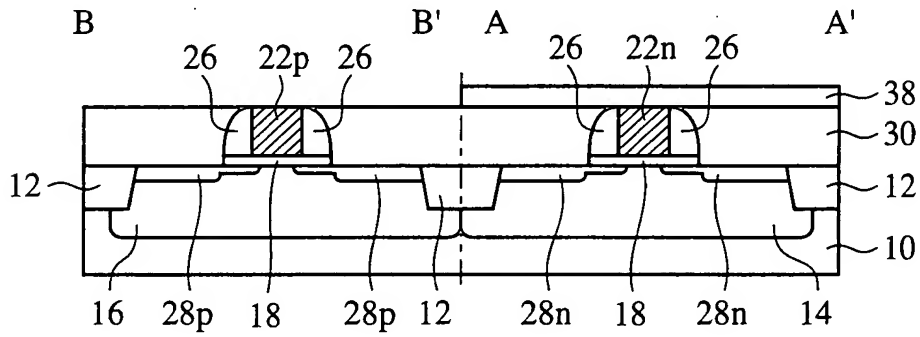
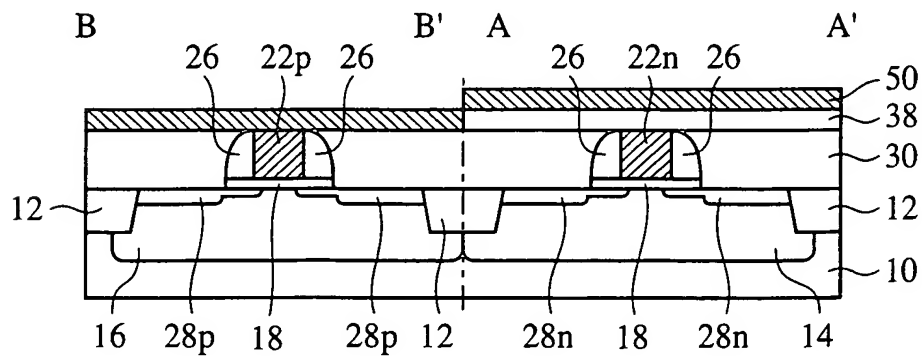


FIG. 19C



20/27

FIG. 20A

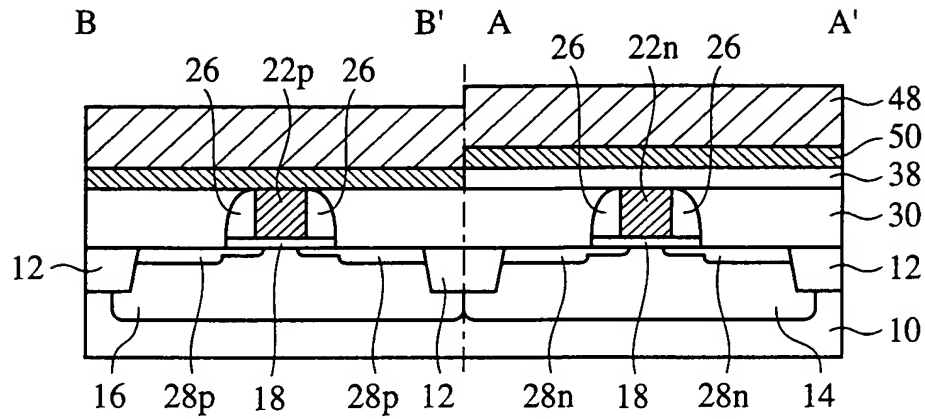


FIG. 20B

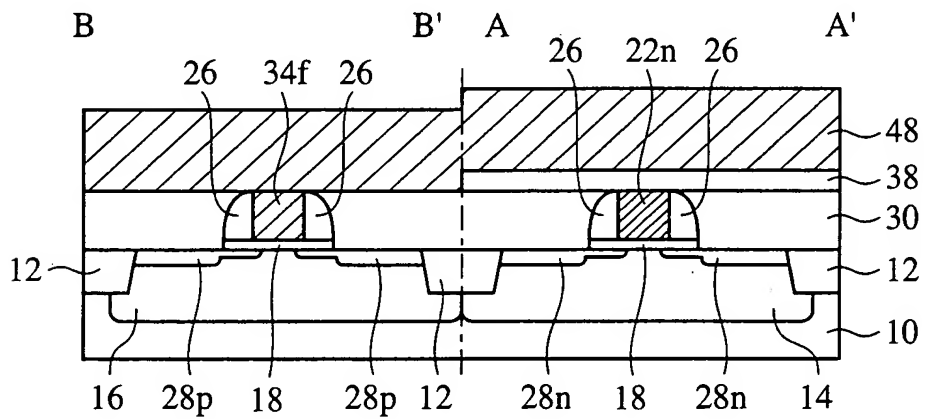
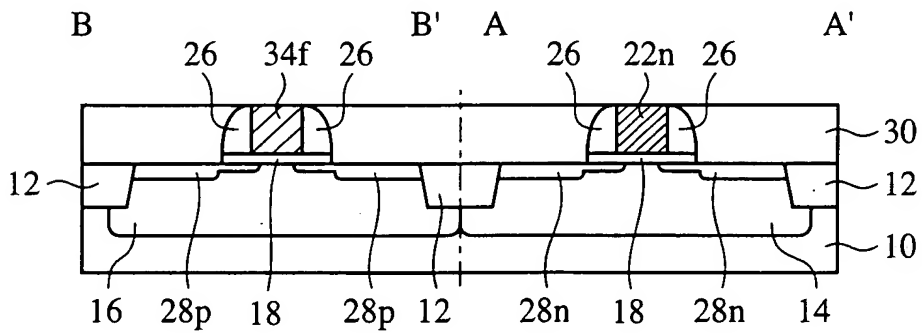


FIG. 20C



21/27

FIG. 21A

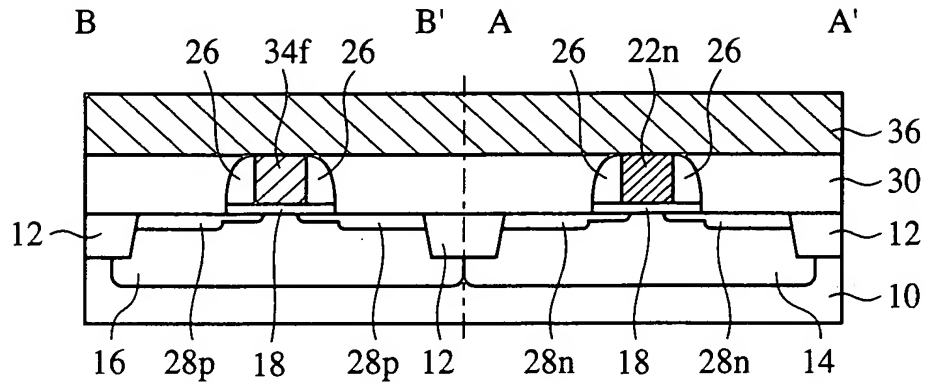


FIG. 21B

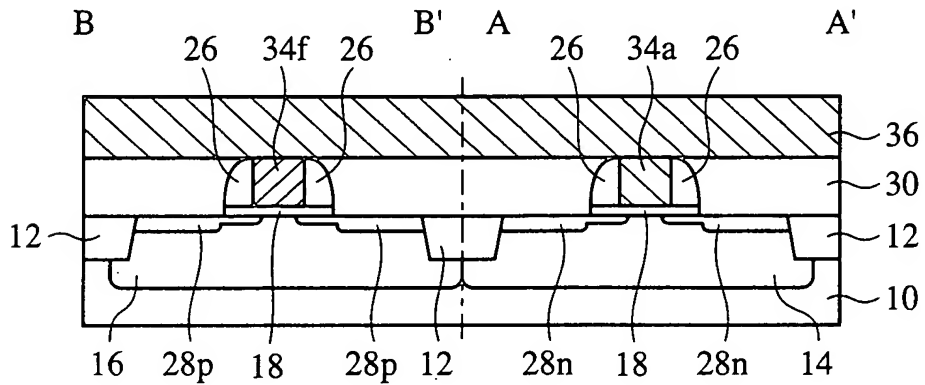
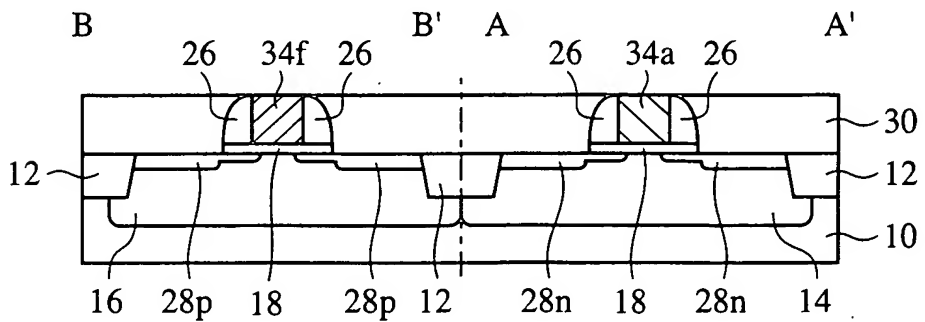
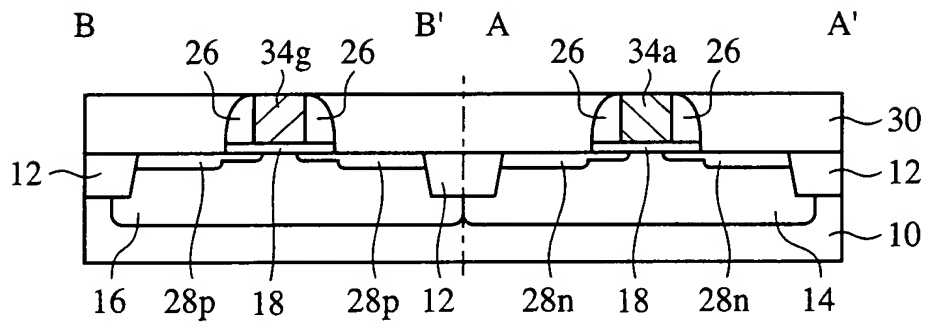


FIG. 21C



22/27

FIG. 22



23/27

FIG. 23A

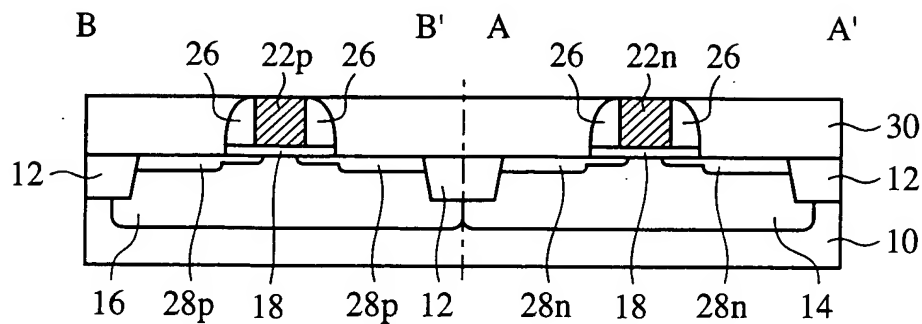


FIG. 23B

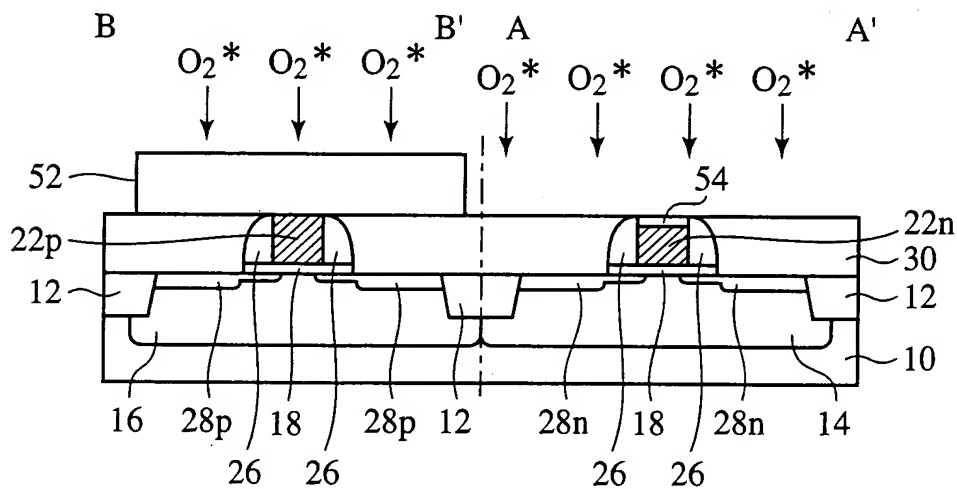
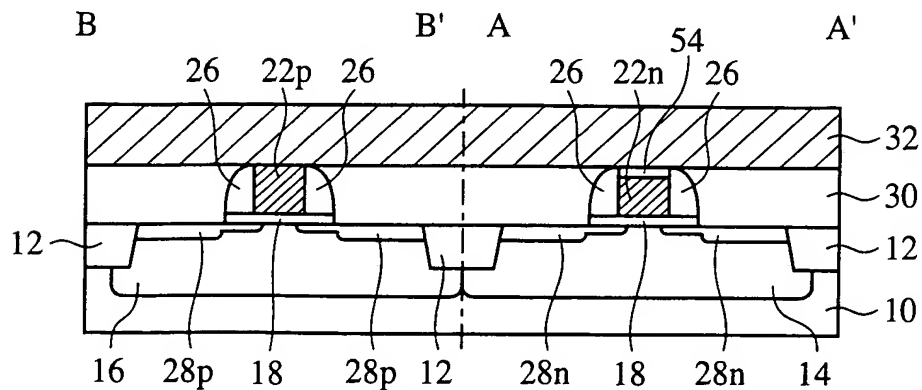


FIG. 23C



24/27

FIG. 24A

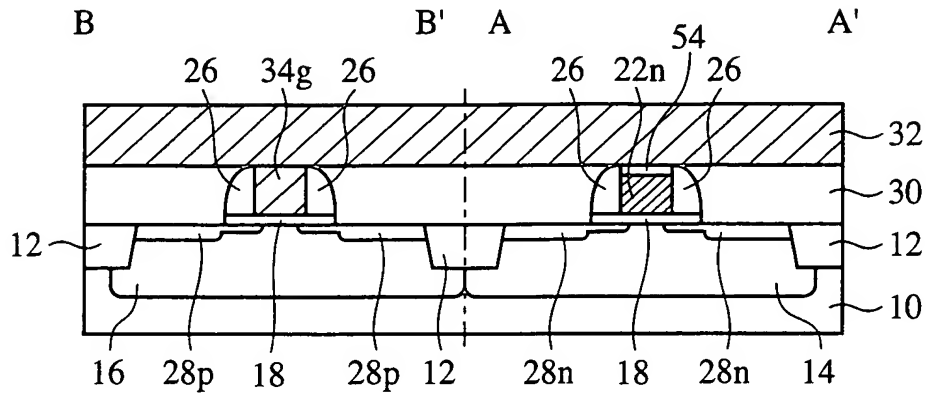


FIG. 24B

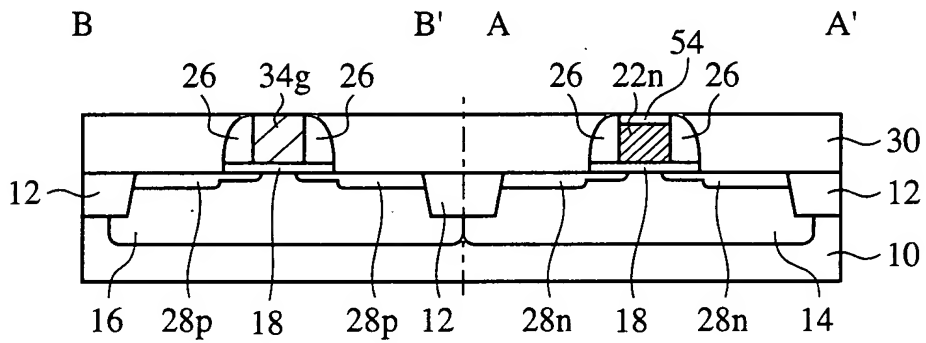
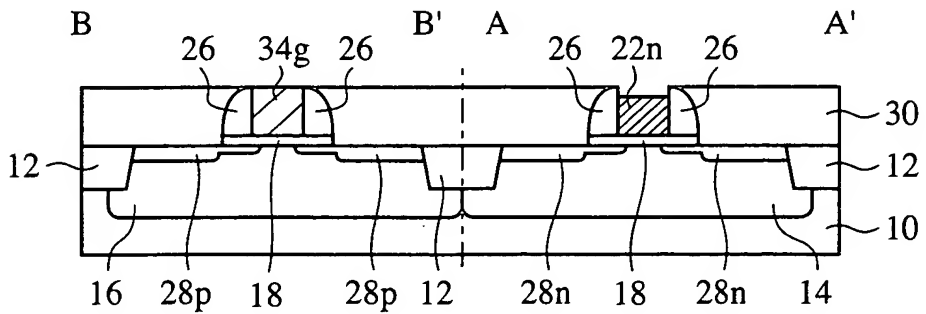


FIG. 24C



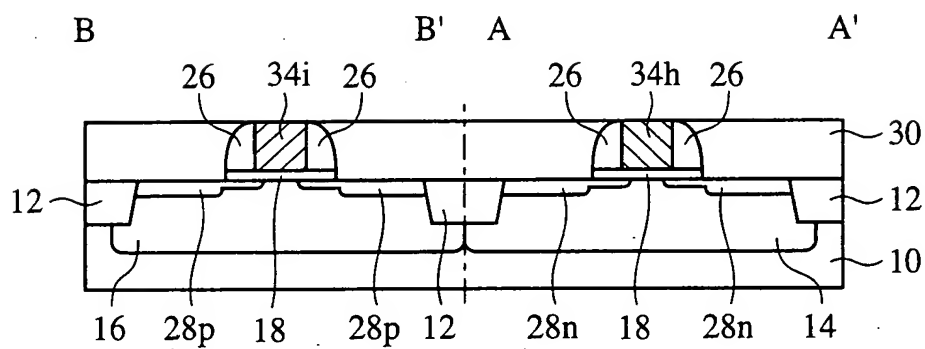


This cross-sectional view shows a semiconductor device with a trench structure. The device includes a substrate 10 with a trench 12. A layer 14 is formed on the bottom surface of the trench 12. A layer 16 is formed on the side walls of the trench 12. A layer 18 is formed on the top surface of the substrate 10. A layer 26 is formed on the top surface of the substrate 10. A layer 30 is formed on the top surface of the substrate 10. A layer 34g is formed on the top surface of the substrate 10. A layer 34a is formed on the top surface of the substrate 10. A layer 36 is formed on the top surface of the substrate 10. The trench 12 is divided into two regions, 28p and 28n, by a dashed line 12. The regions 28p and 28n are separated by a layer 14. The regions 28p and 28n are separated by a layer 16. The regions 28p and 28n are separated by a layer 18. The regions 28p and 28n are separated by a layer 26. The regions 28p and 28n are separated by a layer 30. The regions 28p and 28n are separated by a layer 34g. The regions 28p and 28n are separated by a layer 34a. The regions 28p and 28n are separated by a layer 36.

A cross-sectional view of a semiconductor device. The diagram shows several horizontal layers labeled 10, 12, and 30 from bottom to top. A central vertical dashed line separates two symmetrical halves. On the left side, there are regions labeled B, B', and A. On the right side, there are regions labeled A'. Various numerical labels indicate specific features or dimensions: 16, 28p, 18, 28p, 12, 28n, 18, 28n, and 14 along the bottom; 26, 34g, 26, 26, 34a, 26 along the top; and 12, 30, 12, 10 along the right edge.

26/27

FIG. 26



27/27

FIG. 27A

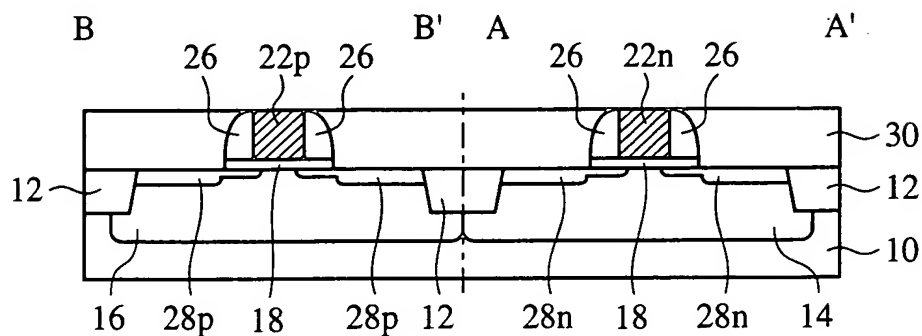


FIG. 27B

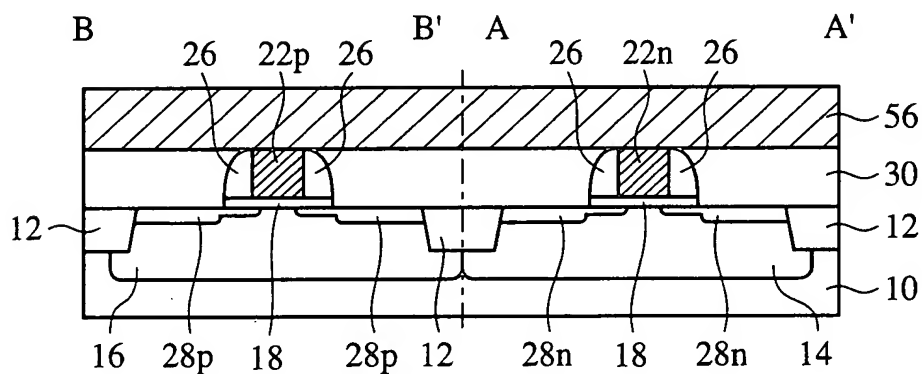


FIG. 27C

